ANALOG DEVICES

AN-405
APPLICATION NOTE

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Increasing the Speed of the Output Response of the AD606

by Peter Checkovich

INTRODUCTION

The AD606 is a complete demodulating logarithmic amplifier. As such it incorporates successive detection stages, a dc feedback section to null out the input offset voltage, a current summer to add up the logarithmic current outputs of the stages, and a low pass filter for the log output to remove the carrier from the demodulated signal. The latter, while offering useful integration for some lower speed systems, slows down the response of the logarithmic output in high speed systems. It is therefore desireable in high speed systems to bypass this filter and realize the faster response.

The higher speed response is important when using the AD606 as a logarithmic detector for systems like medical ultrasound where it is desired to observe a weak echo signal that closely follows a strong echo signal. It is imperative that the response of the log detector to the strong echo to totally decay before the following weak signal can be detected accurately.

The intent of this application note is to describe how to realize a speed up of approximately a factor of eight in the logarithmic output response of the AD606.

The internal block diagram of the AD606 as it appears in the data sheet is shown in Figure 1. The various blocks mentioned above are all shown. It can be seen that the

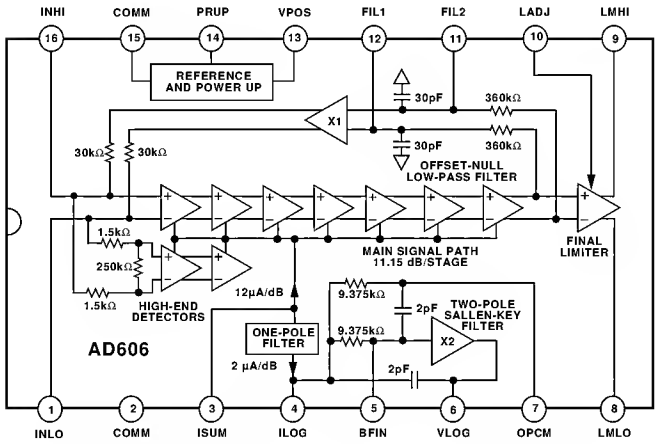

Figure 1. AD606 Simplified Block Diagram

detected current from all the successive demodulating stages is low pass filtered, converted to a voltage and output to VLOG (Pin 6). However, one node called ISUM is connected to Pin 3 and no other mention of it is made in the data sheet. However, all applications show this pin as an N/C, so it is not obvious how to get useful current from this node.

The key to steering the current available at the ISUM node (labeled as 12 µA/dB) to Pin 3, is to bias Pin 3 at the same voltage as the positive supply of the AD606 (VPOS, Pin 13). This will steer the current away from being internally consumed in the part and direct it off chip. This current into Pin 3 can then be converted to a voltage by using an op amp I to V converter.

There is, however, an accuracy penalty that is incurred by using this technique. The ISUM current is inversely proportional to the value of a thin film resistor whose absolute accuracy is ±25%. The thin film resistors used in the on-chip I to V circuitry match those of the ISUM circuit by better than 1% so the overall accuracy is not adversely affected when using the on-chip I to V converter.

When using the faster off-chip I to V converter, the ±25% tolerance of the thin film resistors of the AD606 will affect the gain of the logarithmic output. In systems where linearity is most important and the system is calibrated for overall gain variations, this should not present any problems.

The off-chip I to V converter will also have a slightly greater variation in the intercept vs. temperature than the on-chip I to V converter. Once again, the therrmal tracking properties of the thin film resistors minimizes the thermal variations in the AD606, while using an off-chip I to V converter will have about 1 dB of additional variation in the intercept.

Two configurations can accomplish the proper biasing of the ISUM terminal as described, however, each requires an additional power supply. Since the AD606 is a single supply part, the price for the added performance comes at the expense of added system complexity.

ALL POSITIVE SUPPLY CONFIGURATION

The first configuration uses a +5 V and ground supply for the AD606 as the part is normally designed to operate. Since ISUM will now want to be operating at +5 V, a higher supply voltage, nominally +10 V, will be required for the I to V converter. Figure 2 is a schematic of this configuration. This configuration lends itself well to battery powered systems, where supplies of only one polarity are available and a dc to dc converter to create a negative supply would generate too much noise.

The positive input of the op amp is biased at +5 V. The feedback circuit of the op amp will drive the inverting input to also be biased at +5 V, which is the point it wants to operate at to use the current available at ISUM as explained above.

For high speed response, a high speed op amp like one from Analog Devices XFCB process is required. If filtering of the carrier frequency from the response is also to be incorporated by using a capacitor in shunt with the feedback resistor, then the op amp will have to be a voltage feedback type. Also because the op amp is configured with 100% feedback, a unity gain stable op amp is required. Candidates that meet these criteria and are cost effective and low power consumption are the AD8041 and AD8047.

The value of the feedback resistor for the op amp will determine the scaling of the output. The current into the ISUM node is 12 μA/dB. In order to produce the same response as the AD606 (37.5 mV/dB) the feedback resistor should be 37.5 mV/12 μA or 3.12k. Over the 80 dB range of the AD606, this will produce a signal with a dynamic range of 80 dB × 37.5 mV/dB or 3.0 V.

Another factor to consider is that with no signal at the input of the AD606 and ISUM biased at the same potential as the positive supply of the AD606, the standing current into ISUM is 650 μA dc. This current will create a voltage of 2.0 V across a 3.12k feedback resistor with the output more positive than the inverting input. Thus, the op amp will have a baseline output of 7 V (5 V + 2 V) and will want to go 3 V higher than this to handle the dynamic range of the signal. With a positive rail of only +10 V, this is not possible.

One approach is to reduce the value of the feedback resistor by a factor of two resulting in a value of 1.54 k (nearest 1% value). This will cut the generated voltages described above in half and yield half the scale factor for the log output (18.75 mV/dB). Thus the baseline output will be 6 V and the dynamic range of the signal will be 1.5 V. This will generate a signal that at its maximum is

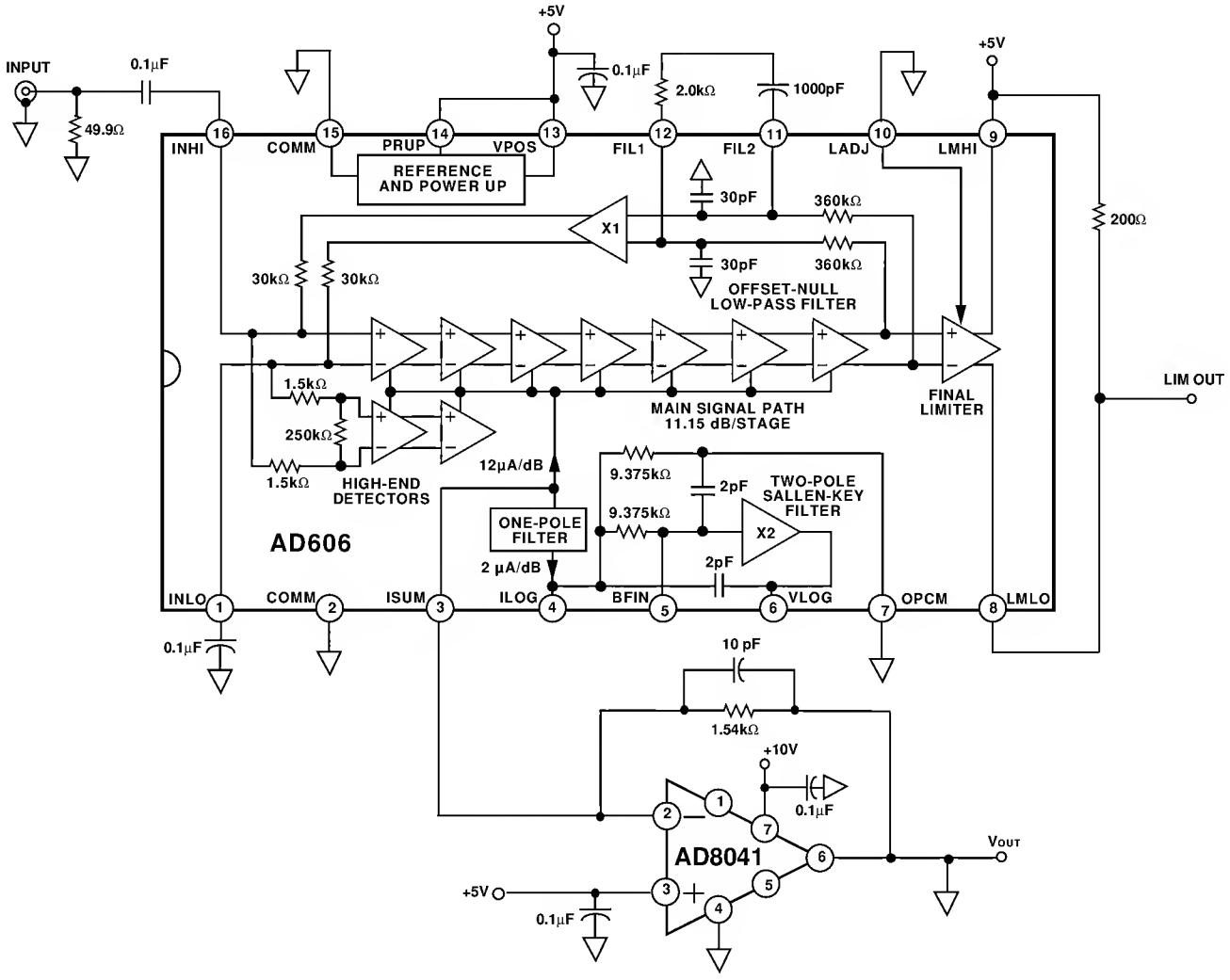

Figure 2. 0 V, +5 V +10 V Configuration

2.5 V below the positive rail of the op amp. Another technique for shifting the baseline dc level at the output of the op amp will be discussed in the next section.

Figure 3 shows the response of the AD8041 output of the circuit in Figure 2. The input signal is a sinusoidal burst at a frequency of 10.7 MHz and an amplitude of 10 mV p-p. The 10 pF capacitor across the feedback resistor was selected to provide the best compromise between filtering the carrier ripple and minimizing the rise and fall times of the output. In comparison Figure 4 shows the VLOG output of the AD606 as conventionally operated using the same input signal. It can be seen that by using the speed up technique the rise and fall times have decreased from approximately 400 ns to 50 ns or about a factor of eight improvement. Other signal amplitudes of 1 mV, 100 mV and 1 V p-p were also used as an input with similar results.

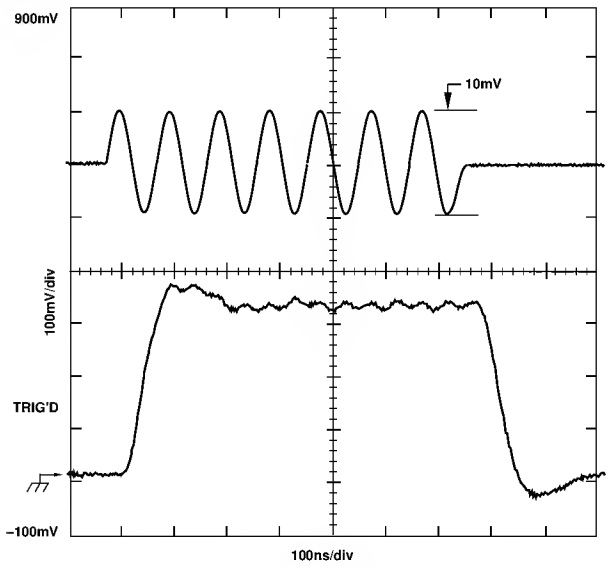

Figure 3. V_{OUT} Response of the Circuit in Figure 2

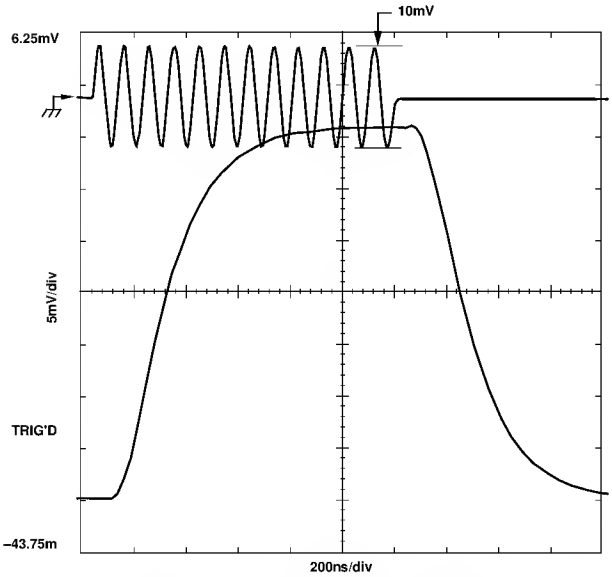

Figure 4. V_{LOG} Response of AD606

DUAL SUPPLY CONFIGURATION

If the baseline output of the op amp is desired to be at or near ground, then the supplies for the AD606 can be shifted down by 5V so that it operates with ground as its most positive rail and -5V as its lower rail. All other pins of the AD606 that are normally directly connected to a power supply must also be shifted down by 5V from the standard connections. This will change the location of the bypass capacitors. The pins that are newly assigned to -5V require bypass capacitors (to ground), while those newly assigned to ground do not. In single-ended circuits, an undriven input to the AD606 can still have its capacitor connected to ground in this configuration.

With the top rail of the AD606 at ground, ISUM also wants to be biased at ground. So besides the ground and -5V supplies, an additional +5V supply is required to power the op amp I to V converter. Fig. 5 is a schematic of this configuration. The non-inverting input of the op amp is biased at ground which forces the inverting input (and ISUM) to also be at ground.

The dc standing current into ISUM will create a baseline voltage of 1V (650 μA x 1.54K) at the output of the op amp. More operating headroom in the op amp can be obtained if this voltage can be shifted down. Providing current into the summing node can accomplish this voltage shift.

If it is desired to shift this voltage down by 1V (for a baseline voltage at ground), then a current of 1V/1.54k or 650 μA will have to be input into the summing node. If the +5V supply is used to provide this current, then R1 should be 5V/650 μA or 7.68k (nearest 1% value). Fig. 5 shows the location of this resistor in the circuit. This assumes that the +5V supply is accurate enough for this application. For greater accuracy, a voltage reference can be used and similar calculations performed to obtain the proper component values. This same technique for level shifting the baseline output of the op amp can be used in the all positive supply configuration described above.

If the intrinsic 37.5 mV/dB scaling of the AD606 is desired, then the feedback resistor can be increased to 3.16k. As mentioned above, this will create a signal with a 3V dynamic range which requires more headroom. The AD8041 can handle a 0 to 3V single with a +5V positive rail, but to use op amps with less headroom like the AD8047, the baseline can be shifted further negative to provide more operating headroom. In general, downstream circuitry will dictate the desired dynamic range and dc operating point.

CONCLUSIONS

The methods presented above increase the speed of the logarithmic output response of the AD606 by approximately a factor of eight over the response of the integrated output circuit. A high speed op amp I to V converter replaces the intrinsic op amp in the AD606 to provide the improved response. The slope and intercept variations are affected, but can be compensated in some systems. Two power supply configurations are described along with techniques for varying the scale factor and the dc operating point of the output.

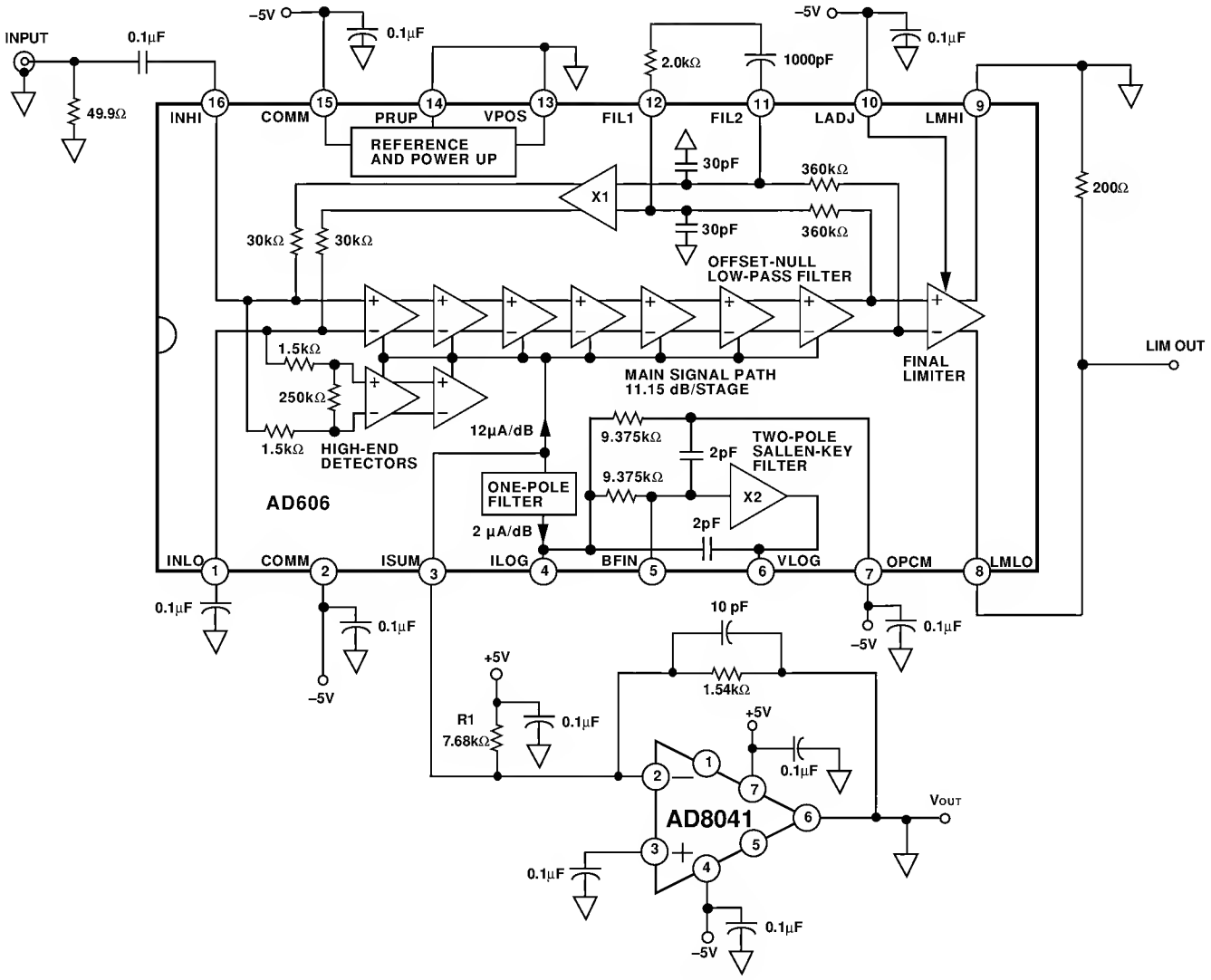

Figure 5. –5 V, 0 V, +5 V Configuration